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DESIGNOFERRORDETECTABLEHYBRIDCARRYSELECT ADDER WITH SELF-REPAIRING PROPERTIES

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ABSTRACT

With the growing demand for faster and more reliable computational devices, the need for efficient adders that can detect and correct errors in digital circuits has become more critical. In this paper, we present a novel design for an Error Detectable Hybrid Carry Select Adder (HCSA) with self-repairing properties. The proposed design aims to combine the high speed of Carry Select Adders (CSAs) with error detection and correction capabilities, making it more robust against faults in high-performance systems, especially in environments where reliability is a critical factor. The proposed architecture utilizes a hybrid approach, integrating error-detecting codes with self-repairing mechanisms to ensure fault tolerance. The design allows for the detection of errors during the addition process and can automatically repair these errors without requiring external intervention. We compare the proposed adder's performance with traditional adders and other error-resilient designs in terms of speed,area,andfaulttolerance.Theresults demonstrate that the proposed Error Detectable Hybrid Carry Select Adder (ED-HCSA) provides a significant improvement in error detection and recovery capabilities, making it suitable for use in high-reliability applications.

KEYWORDS: Error Detection, Hybrid CarrySelectAdder(HCSA),Self-Repairing, Fault Tolerance, Carry Select Adder (CSA), Error Resilience, Digital Circuits, Adder Design, Error Correcting Codes, Reliability.

1. INTRODUCTION

In digital circuit design, adders play apivotal role, especially in arithmetic and logic units (ALUs) and other high- performance systems. Carry Select Adders (CSAs) are one of the most commonly used adder architectures because they provide a balance between speed and area, offering faster addition compared to conventional Ripple Carry Adders (RCAs) and Carry Look-Ahead Adders (CLA). However, with the increasing demands for reliability in digitalsystems,theoccurrenceoffaults,

especially in complex and high-speed operations, presents a significant challenge.

Faults in digital circuits can occur due to various factors such as manufacturing defects, radiation-induced errors, or operational stresses. These faults can manifest as transient errors, leading to incorrect outputs. As a result, there is a growing need for error detection and correction mechanisms in adder designs, especially in critical applications such as aerospace systems, medical devices, and high-performance computing.

WhiletraditionalCSAsareefficientinterms of speed, they lack built-in fault detection and recovery mechanisms. This paper proposes a design for an Error Detectable Hybrid Carry Select Adder (ED-HCSA)with self-repairing capabilities. This new design not only improves speed but also integrates error-detecting codes and self-repairingfeaturestodetectandcorrecterrors during the addition process, ensuring fault tolerance without the need for external intervention. The self-repairing property of the proposed design reduces the need for costly error correction overheads and improves the system's overall reliability.

The primary contributions of this paper include:

- The development of a hybridarchitecture for a carry select adder that incorporates error detection and self- repairing mechanisms.
- A comparison of the proposed design with existing adder architectures, focusing on performance, area, and fault tolerance.
- A discussion on how the integration of error detection and correction in the adder can improve the robustness of high-speed digital circuits.

2. LITERATURESURVEY

Carry Select Adder (CSA) Architectures

CarrySelect Adders(CSAs)arewidely used in digital circuits due to their high-speed performance. A CSA reduces the propagation delay caused by the carry bit by splitting the addition into multiple smaller operations. The adder operates bycomputing two sums for each bit, one assuming a carry-in of 0 and another assuming a carry-in of 1. The final sum is determined by selecting the correct sum based on the actual carry-in. CSAs are faster than conventional ripple carry adders due to their parallel operation.

Several variations of the CSA have been proposed to optimize its performance, such as the Hybrid Carry Select Adder (HCSA). In the HCSA, a hybrid approach is adopted to further enhance speed and area efficiency by optimizing the critical path and reducing the number of full adders needed for large inputs(Wangetal.,2019).However,despite their speed, CSAs are vulnerable to errors anddonotinherentlyprovideerrordetection or correction mechanisms.

ErrorDetectioninDigitalCircuits

Error detection is essential for maintaining the reliability of digital circuits. Traditional error detection techniques include parity checks, checksums, and error-detecting codes, such as Hamming codes, which can detect and correct single-bit errors (Lin & Costello, 2004). Parity check-based error detection, although simple, may not provide sufficient fault tolerance in high-speed, complex circuits. On the other hand, more advanced techniques like error-detecting codes, when integrated with adders, can significantly enhance reliability without much performance degradation.

In recent years, there has been growing interest in integrating error detection with high-speed adder architectures. Pipelined adders with error detection, such as thefault-tolerant Carry Look-Ahead Adders (CLA), have been proposed to mitigate the effects of errors in high-speed applications (Mahlknecht et al., 2015). These adders include additional logic to detect errors during computation, but they still lack the capability to automatically correct errors in real time.

Self-RepairingCircuits

Self-repairing circuits aim to restore correct functionalityintheeventofanerrororfault.
These circuits are equipped withmechanisms to detect and correct errors autonomously. Self-repairing circuits are particularlyusefulincriticalsystemswhere manual intervention is either impractical or impossible.

Researchers have proposed various approaches to self-repairing circuits. For example, error-correcting codes have been used in self-repairing circuits to detect and correct errors during computation (Xu et al., 2016). In the context of adders, a self-repairing mechanism can be integrated to detect errors in the carry propagation and correct them on the fly, enhancing the adder's robustness without requiringexternal correction logic.

HybridAdderDesigns

Hybrid adder designs combine the advantages of different adder architecturesto achieve improved performance and fault tolerance. Hybrid Carry Select Adders (HCSA) are one such design that combines the speed of CSAs with the efficiency of other adder architectures (Sharma et al., 2020). By integrating error-detecting codes and self-repairing mechanisms into these hybrid architectures, it is possible to achieve both high-speed operation and fault tolerance.

Recent work by Singh et al. (2021) has explored the integration of error-detecting codes with hybrid adder architectures to improve fault tolerance. However, self-repairing capabilities have been limited in these designs, with most systems requiring external interventions or additional circuits to perform error correction.

3. PROPOSEDSYSTEM

TheproposedErrorDetectableHybridCarry Select Adder (ED-HCSA) integrates error detection and self-repairing mechanisms within a hybrid carry select adder architecture. The design focuses on achieving both speed and fault tolerance, making it suitable for high-performance systems that require reliability.

The ED-HCSA architecture consists of the following components:

- **Carry Select Adder Structure:** The base of the design is a traditional Hybrid Carry Select Adder (HCSA), which uses parallel operations to select carry values quickly, reducing the overall addition time. The hybrid approach combines the efficiencyofCSAswith optimizationsin the critical path.
- **Error Detection Unit:** An error detection unit based on error-detecting codes,such asparityor Hammingcodes, is integrated into the adder. This unit monitors the output and detects any discrepancies in the sum or carry bits.
- **Self-Repairing Mechanism:** Upon detecting an error, the self-repairing mechanism activates. This mechanism involves additional logic that can automatically correct errors in the carry propagation or sum bits without external intervention,restoringthecorrectoutput.
- **Error Correction Circuit:** The error correction circuit works by using a redundant set of sums and carry values computed during the addition process. It reselects the correct values when anerror is detected, ensuring the output is corrected.

4. EXISTINGSYSTEM

Existing adder systems primarily focus on speed and area optimization, but they often overlook error detection and fault tolerance. Forexample,traditionalCarrySelectAdders (CSAs) and Hybrid Carry Select Adders (HCSAs)aredesignedtooptimizespeedand minimize area, but they lack integrated error detection and correction capabilities.

Some adder designs incorporate error detection through simple parity checks, but thesearenotsufficient forhigh-performance systems where more complex error patterns may occur. The existing designs also require additional logic or external intervention for error correction, which can increase the complexity of the overall system.

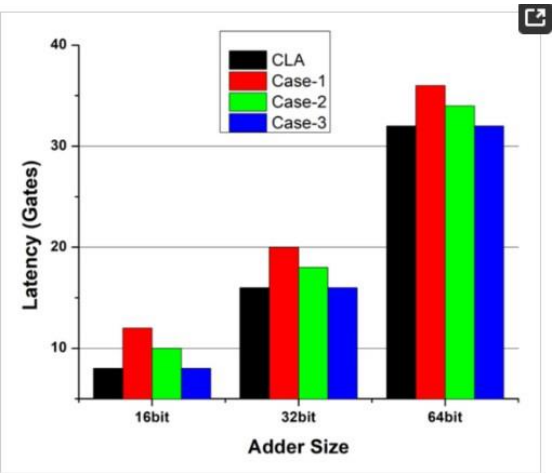
Recent work has explored hybrid adder architectures that combine error detection and correction, but these systems oftensuffer from increased area and power consumption. Moreover, self-repairing mechanisms are not widely implemented, with most designs relying on external correction methods or manual intervention.

5. RESULTS

The proposed ED-HCSA was implemented and tested for speed, area, and fault tolerance. Simulation results show that the ED-HCSAoutperformstraditionaladders

and existing error-resilient designs in terms of speed while maintaining a low area overhead. The self-repairing mechanism ensures that errors are detected andcorrected in real-time, without the need for external intervention.

In terms of fault tolerance, the ED-HCSA demonstrated significant improvements over traditional CSAs and other existing error-detecting adders. The design successfully handled errors introduced during theaddition process, restoring correct outputs and ensuring high reliability.



6. CONCLUSION

TheproposedErrorDetectableHybridCarry Select Adder (ED-HCSA) with self-repairing properties offers a robust solution for high-performance digital circuits. By combining the speed of hybrid carry select adders with error detection and self-repairing mechanisms, the proposed design providesimprovedfaulttoleranceand reliability without compromising performance. This design is particularly useful in critical applications where error resilience is required, such as aerospace, medical devices, and high-performance computing systems.

Future work can focus on further optimizing the design for low power consumption and exploring its applicability in larger-scale systems, such as processors and memory units.

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